Features

3 input reference clocks:

- Two differential clock pair up to 1GHz, accepting single-ended clock source up to 350MHz
- One crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source

4 output clocks:

- Two power banks with 2 differential outputs each, supporting LP-HCSL only
- One independent LVCMOS output clock

Frequency range:

- LP-HCSL: DC to 1GHz
- LVCMOS: DC to 350MHz

Excellent PSRR :-76dBc (LP-HCSL) @ 156.25MHz

Ultra-low latency and skew

Additive Jitter:

- 34 fs RMS (12kHz to 20MHz) typical @LP-HCSL 156.25MHz
- 10 fs RMS typical @ PCIe Gen5 jitter (CC)

Configurable power supplies:

- Core: 1.8V-3.3V
- Differential outputs
- Single-ended outputs

Pin-based control for flexible input reference selection and output enable/disable

Glitch-free switchover supported in the "G"version

Working temperature: -40°C to +85°C

Package: 32-pin WQFN

1.SYKB*****: No glitch-free switchover.
2.SYKB*****G: Includes glitch-free switchover.
3.H: Supports LP-HCSL differential clock output only.
4.Unless otherwise stated, the terms "clock buffer" and "buffer" refer to the entire series.

General Description

SYKB23H04(G)[1,2,3,4] is a type of high-performance clock fanout buffer operating at up to 1GHz with 4 outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation.

The buffer supports clock input selection from either two differential clock pairs or one crystal input, distributing the selected clock to two output banks, each with 2 differential outputs, along with a dedicated LVCMOS output. Both differential output banks can be configured as LP-HCSL or disabled (HiZ).

Operating with a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, the clock buffer provides flexible control via logic pins for input reference clock selection and output enable/disable functions.

The buffer can be paired with SYNK Technology’ s SYKG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Applications

PCIe® 1.0 to 6.0 and NVLink

Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards

Servers, storage systems, switches, routers, and display panels

Reference clock distribution for BBU and RRU applications

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