

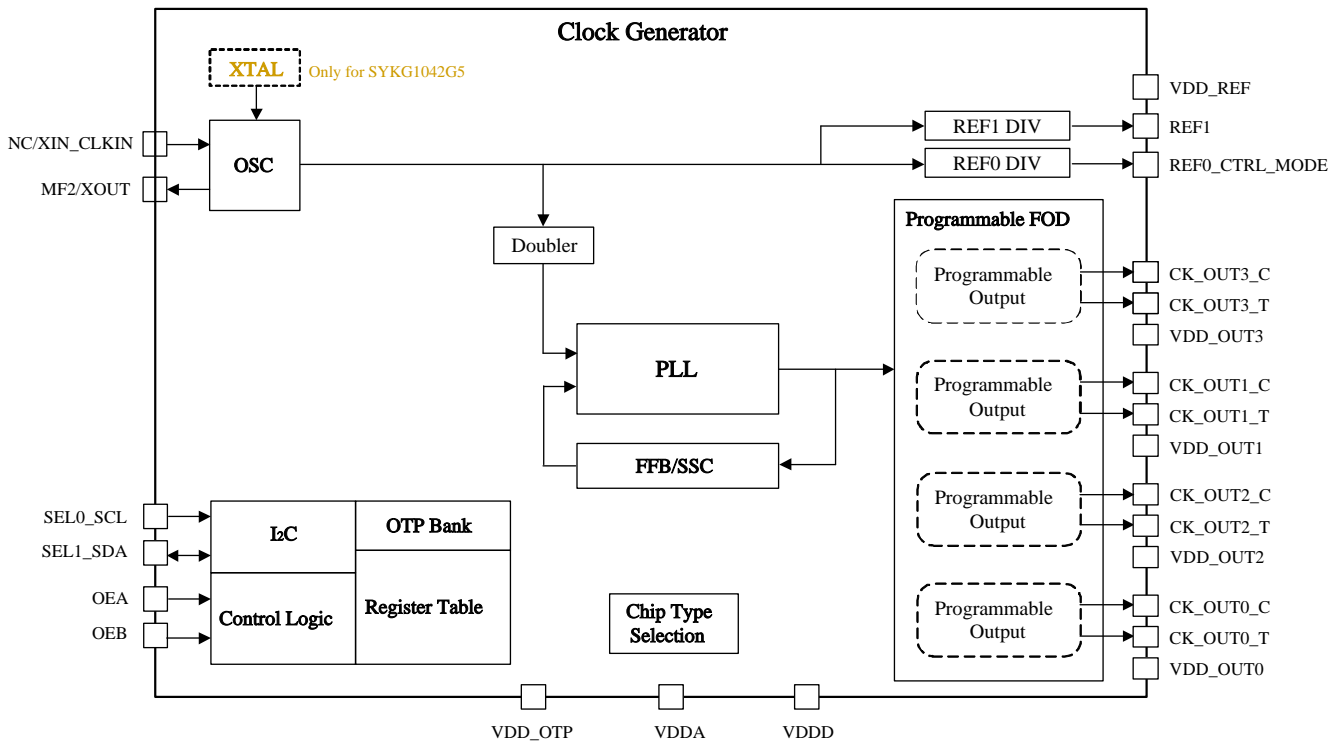


SYKG1042E/Q5

Features

Functional Block Diagram

Figure 1. SYKG1042E/Q5 Block Diagram



Notes:

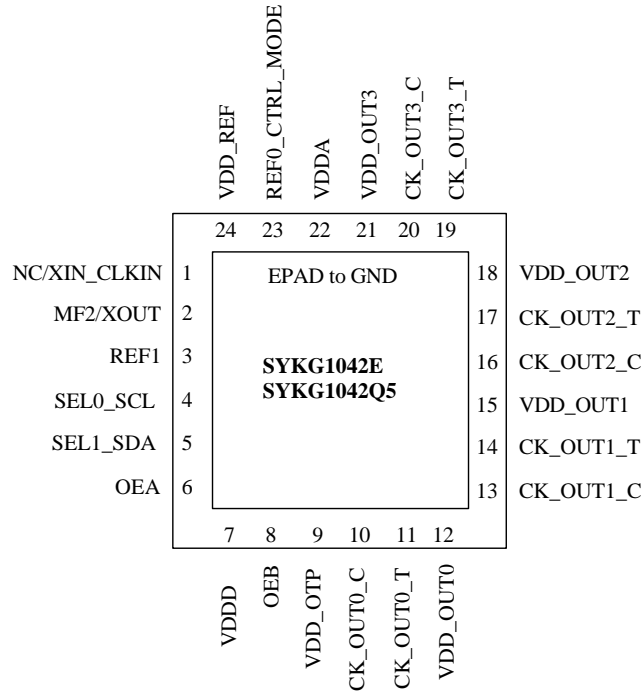
1. FFB: Fraction Feedback Divider
 FOD: Fraction Output Divider
 IN DIV: Input Divider
 OTP: One-Time Programmable
 PLL: Phase Locked Loop
 SSC: Spread Spectrum Clocking
 XTAL: Crystal



1 Pin Information

1.1 Pin Assignment

Figure 2. 24-VFQFPN / 24-LGA Pin Assignment, 4.0mm x 4.0mm, 0.5mm Pitch (Top view)



1.2 Pin Description

Table 1. Pin Description for SYKG1042E (24-VFPQFN) & SYKG1042Q5 (24-LGA) (Sheet 1 of 2)

| PinNO. | PinName | Type | Description |
|--------|--------------|--------------|--|
| 1 | NC/XIN_CLKIN | Input | Crystal input or reference clock input or multi-function pin. |
| 2 | MF2/XOUT | Input/Output | Crystal output or multi-function pin. |
| 3 | REF1 | Output | LVC MOS reference output. |
| 4 | SEL0_SCL | Input | Tri-state logic clock pin with 120k internal pull-up and pull-down. Be used as LSB of control mode selection or I2C SCL. |
| 5 | SEL1_SDA | Input/Output | Tri-state logic data pin with 120k internal pull-up and pull-down. Be used as MSB of control mode selection or I2C SDA. |
| 6 | OEA | Input | Active High input for enabling outputs. This pin has internal 120k pull-up resist or, and works with OEB. |
| 7 | VDDD | Power | Digital power. Connect to 1.8V, 2.5V, 3.3V. |
| 8 | OEB | Input | Active High input for enabling outputs. This pin has internal 120k pull-up resist or, and works with OEA. |

Table 1. Pin Description for SYKG1042E (24-VFPQFN) & SYKG1042Q5 (24-LGA) (Sheet 2 of 2)

| Pin NO. | Pin Name | Type | Description |
|---------|----------------|---------------|---|
| 9 | VDD_OTP | Power | Voltage for OTP programming, $1.8V \pm 10\%$. For Read operation, this pin can be connected to VDDD if VDDD is lower than 2.5V. This pin must be tied to ground or floating if the VDDD is greater than 2.5V. It is recommended to connect VDD_OTP to ground or leave VDD_OTP floating, no matter what level VDDD is. |
| 10 | CK_OUT0_C | Output | Complementary Output Clock0. |
| 11 | CK_OUT0_T | Output | Output Clock0. |
| 12 | VDD_OUT0 | Power | Power supply for Output Clock0. |
| 13 | CK_OUT1_C | Output | Complementary Output Clock1. |
| 14 | CK_OUT1_T | Output | Output Clock1. |
| 15 | VDD_OUT1 | Power | Power supply for Output Clock1. |
| 16 | CK_OUT2_C | Output | Complementary Output Clock2. |
| 17 | CK_OUT2_T | Output | Output Clock2. |
| 18 | VDD_OUT2 | Power | Power supply for Output Clock2. |
| 19 | CK_OUT3_T | Output | Output Clock3. |
| 20 | CK_OUT3_C | Output | Complementary Output Clock3. |
| 21 | VDD_OUT3 | Power | Power supply for Output Clock3. |
| 22 | VDDA | Power | Analog power. Connect to the same voltage as VDDD with suitable filtering. |
| 23 | REF0_CTRL_MODE | Strapping Pin | Chip configuration model selection and LVCMOS clock output. Tri-state logic input pin. At power-up, the state of this pin is latched to select the functionality of several hardware pins. After power-up, this pin acts as one LVCMOS reference output with the output frequency same as input reference or scale down to 1/64 at most. |
| 24 | VDD_REF | Power | Power supply for REF outputs and the internal XOUT. Nominal voltages are 1.8V, 2.5V and 3.3V. |
| 25 | EPAD | GND | Connect to ground. |

2 Mechanical Package Data

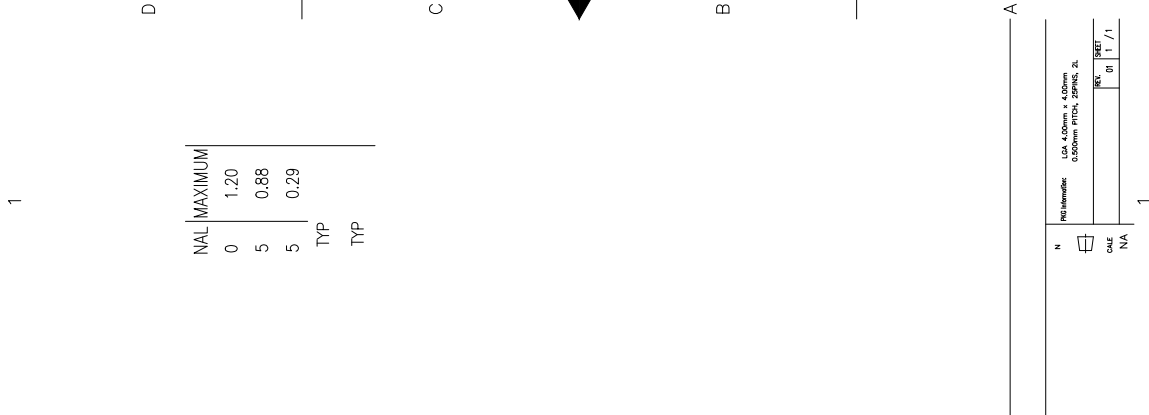
Figure 3. 24-VFQFPN Package Outline (4.0mm x 4.0mm x 0.75mm, 0.5mm Pitch)

| D | | B | | A | |
|-----------------------------|-------|------|------|------|------|
| ↓ | | | | | |
| DIMENSIONS = MILLIMETER) | NOM | 0.75 | 0.02 | 0.25 | 4.00 |
| | MAX | 0.80 | 0.05 | 0.30 | 4.10 |
| | 03REF | 0.02 | 0.05 | 0.25 | 4.00 |
| | 03REF | 0.25 | 0.02 | 0.30 | 4.10 |
| | 03REF | 4.00 | 0.02 | 2.50 | 2.60 |
| | 03REF | 4.00 | 0.02 | 2.50 | 2.60 |
| | 03REF | 2.50 | 0.02 | 0.50 | 0.60 |
| | 03REF | 2.50 | 0.02 | 0.50 | 0.60 |
| | 03REF | 0.40 | 0.08 | 0.45 | 0.08 |
| | 03REF | 0.08 | 0.08 | 0.45 | 0.08 |

ARD MO-220 WGGD-8.
DIMENSIONS.

REV. 1/1
SHEET 1/1

Figure 4. 24-LGA Package Outline (4.0mm x 4.0mm x 1.10mm, 0.5mm Pitch)



3 Ordering Information

| Part Number | Package | Temperature | Crystal | Packing |
|-----------------|--|-------------|----------------|-------------|
| SYKG1042E-XX | 4mm x 4mm x 0.75mm, 0.5 pitch 24-VFQFPN; MSL Level-3-260C | -40 ~ +85°C | External | Tray |
| SYKG1042E-XX-T | | | | Tape & Reel |
| SYKG1042Q5-XX | 4mm x 4mm x 1.10mm, 0.5 pitch 24-LGA; MSL Level-3-260C | -40 ~ +85°C | 50MHz Internal | Tray |
| SYKG1042Q5-XX-T | | | | Tape & Reel |

For more information on the product, please contact <https://www.yxc.hk>