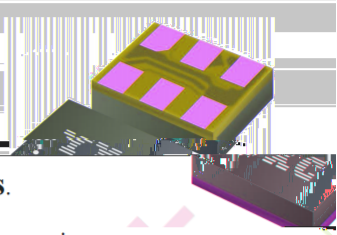
# Crystal Oscillator

# YSO212PU

## General Description（概述）

**YSO212PU is a programmable, low-jitter differential crystal oscillator.**Output frequency is factory programmed as per customer requirements between **200 kHz to 1.5 GHz**. YSO212PU is a low Noise PLL with Integrated XTAL which provides clocks with Jitter of **69 fs**.



With on-chip NVM and factory programming, we can service customer requirements with very fast lead times.

## Features（产品特性）

- Available with any frequency from 200 kHz to 1.5 GHz
- Low Jitter: 69fs@156.25MHz Typ Jrms,12 kHz – 20 MHz
- 26fs Typ Jrms,12 kHz – 20 MHz with 4 MHz HPF
- Fractional N fully integrated PLL
- 3.3 V, 2.5 V and 1.8 V VDD supply operation
- Programmable output performance for PCIe, LVPECL, HCSL, LP-LVDS, LVDS, Programmable HCSL, AC Coupled CML output options available on all differential output pads
- HCSL, LP-HCSL, LVDS Output driver type frequency supports from 70 MHz to 350MHz
- ±50 ppm stability (-40°C to 85 °C)
- Package Options:Available in 6pin Plastic Package : 3.2*2.5mm,2.5*2.0mm,2.0*1.6mm

## Applications（应用领域）

- 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

# List

## 1 Specifications（规格参数）

Table 1 Electrical Characteristic

| Item/Type | Min | Typ | Max | Remarks |
|---|---|---|---|---|
| Output Frequency Range<br>额定频率范围 | | 200K~1.5GHz | | |
| Supply Voltage<br>电源电压 | 1.71V<br>2.375V | 1.8V<br>2.5V | 1.89V<br>2.625V | Voltage Tolerance ±5% |
| | 3.135V | 3.3V | 3.465V | |
| Current Consumption<br>消耗电流 | | LVPECL 71mA<br>LVDS 53mA<br>LVDS Power-Down 57mA | | |
| | | HCSL 66mA<br>HCSL-LP 50mA | | |
| OE terminal | | Input Voltage<br>输入电压 | | VIH=70% VDD Min<br>VIL=30% VDD Max |
| $F_{CLK} \geq 10$ MHz | | Output Disable Time<br>输出禁用时间 | | 2 us + 3 clock Cycles us |
| | | Output Enable Time<br>输出启用时间 | | 2 us + 3 clock Cycles us |
| | | Operating Temperature Range<br>工作温度 | | -40~+85℃ or specify |
| Total stability includes frequency tolerance(initial accuracy, temperature stability, operating temperature or specify, supply voltage variation and 10 year aging at 25℃)<br>频率偏差 | | Total Stability | | |
| Start-up time<br>启动时间 | | 10ms | | |

Table 2 Absolute Maximum Ratings

| Remarks | Item/Type | Min | Typ | Max |
|---|---|---|---|---|
| 3.63V | Core Supply Voltage<br>核心工作电压 | -0.5V | | 3.63V |
| Relative to GND | Voltage range（All inputs）<br>输入引脚电压范围 | -0.5V | | 3.63V |
| 25℃ | Maximum Junction Temperature in Operation<br>最大工作温度 | | | +125℃ |
| | Storage Temperature Range<br>储存温度 | -55℃ | | +125℃ |
| 2.375V 2.5V 2.625V | Programming Voltage<br>编程电压 | | | |
| 100mA Max | Latch-Up<br>闩锁效应 | | | |
| Human body model: 2000V Max<br>Charged device model: 500V Max | ESD<br>静电防护 | | | |

Notes:
1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

Table 3 Output Clock Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **LVDS Outputs** | | | | | |
| Output Common Mode Voltage | VOCM | VDD=2.5/3.3V | 1.25 | 1.375 | V |
| Clock Output Frequency 时钟输出频率 | Fout | 0.2 | | 1500 | MHz |
| Output Rise/Fall Time 上升下降时间 | Trf | | | 350 | ps |
| Output differential peak 输出差分峰值 | VP | 250 | 500 | 400 | mV |
| | | 250 | 500 | ≤700M | |
| | | | | >700M/<1500M | |
| **LVDS-Boost Outputs** | | | | | |
| Clock Output Frequency 时钟输出频率 | Fout | 0.2 | | 1500 | MHz |
| Output Rise/Fall Time 上升下降时间 | Trf | | | 350 | ps |
| Output differential peak 输出差分峰值 | VP | 800 | | @156.25M | |
| | | 600 | | 950 | mV |
| | | 500 | | 950 | |
| **LVPECL Outputs** | | | | | |
| Output High Voltage 输出高电压 | VOH | VDD=1.8/2.5/3.3V | VDD-0.8 | | V |
| Output Low Voltage 输出低电压 | VOL | | VDD-1.55 | | |
| Clock Output Frequency 时钟输出频率 | Fout | 0.2 | | 1500 | MHz |
| Output Rise/Fall Time 上升下降时间 | Trf | | | 350 | ps |
| Output differential peak 输出差分峰值 | VP | @156.25M | 720 | | mV |
| | | ≤700M | 500 | 950 | |
| | | >700M/≤1500M | 400 | 850 | |
| **HCSL Outputs** | | | | | |
| Output High Voltage 输出高电压 | VOH | VDD=1.8/2.5/3.3V | 0.65 | 0.83 | V |
| Output Low Voltage 输出低电压 | VOL | | -0.3 | 0 | |
| Clock Output Frequency 时钟输出频率 | Fout | 0.2 | | 1500 | MHz |
| Output Rise/Fall Time 上升下降时间 | Trf | | | 350 | ps |
| Far End Termination Output differential peak 输出差分峰值 | VP | @156.25M | 800 | | mV |
| | | ≤700M | 400 | 850 | |

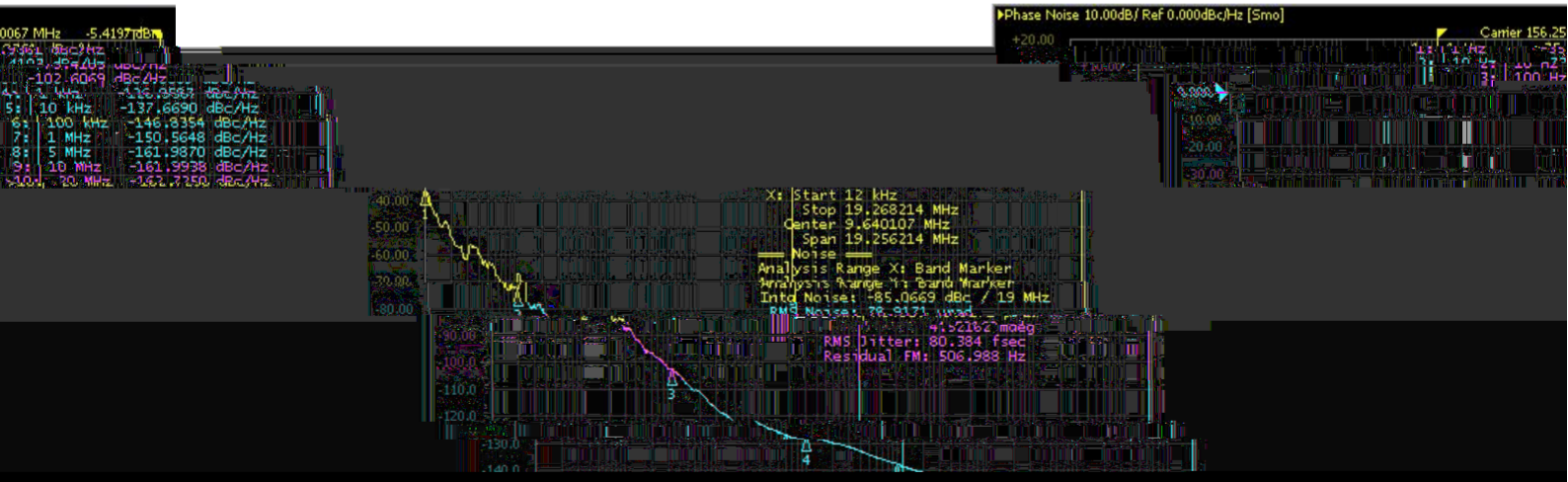
Table 3 (Continued)

| HCSL-LP Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|
| Output High Voltage<br>输出高电压 | VDD=1.8/2.5/3.3V | VOH | 0.7 | 0.8 | 0.9 | | V |
| Output Low Voltage<br>输出低电压 | | VOL | | -0.1 | 0 | 0.1 | |
| Clock Output Frequency<br>时钟输出频率 | | | Fout | 0.2 | | 500 | MHz |
| Output Rise/Fall Time<br>上升下降时间 | | | Trf | | | 350 | ps |
| Output differential peak<br>输出差分峰值 | @156.25M | | VP | | 720 | | mV |
| | ≤500M | | | 500 | | 900 | |

## 1.1 Phase Jitter（相噪抖动）

Table 4 Output RMS Jitter and Phase Noise

| Item/Type | Value | Remarks |
|---|---|---|
| @156.25MHz | RMS Jitter [ 12 kHz ~ 20 MHz ] | 69fs rms Typ. | |
| | RMS Jitter for<br>[ 12 kHz ~ 20 MHz ]Integration Bandwidth with<br>4MHz High Pass Filter | 26fs rms Typ. | |
| | Phase Noise | -35 dBc/Hz@1Hz | |
| | | -73 dBc/Hz@10Hz | |
| | | -102 dBc/Hz@100Hz | |
| | | -126 dBc/Hz@1kHz | |
| | | -137 dBc/Hz@10kHz | |
| | | -146 dBc/Hz@100kHz | |
| | | -150 dBc/Hz@1MHz | |
| | | -161 dBc/Hz@10MHz | |



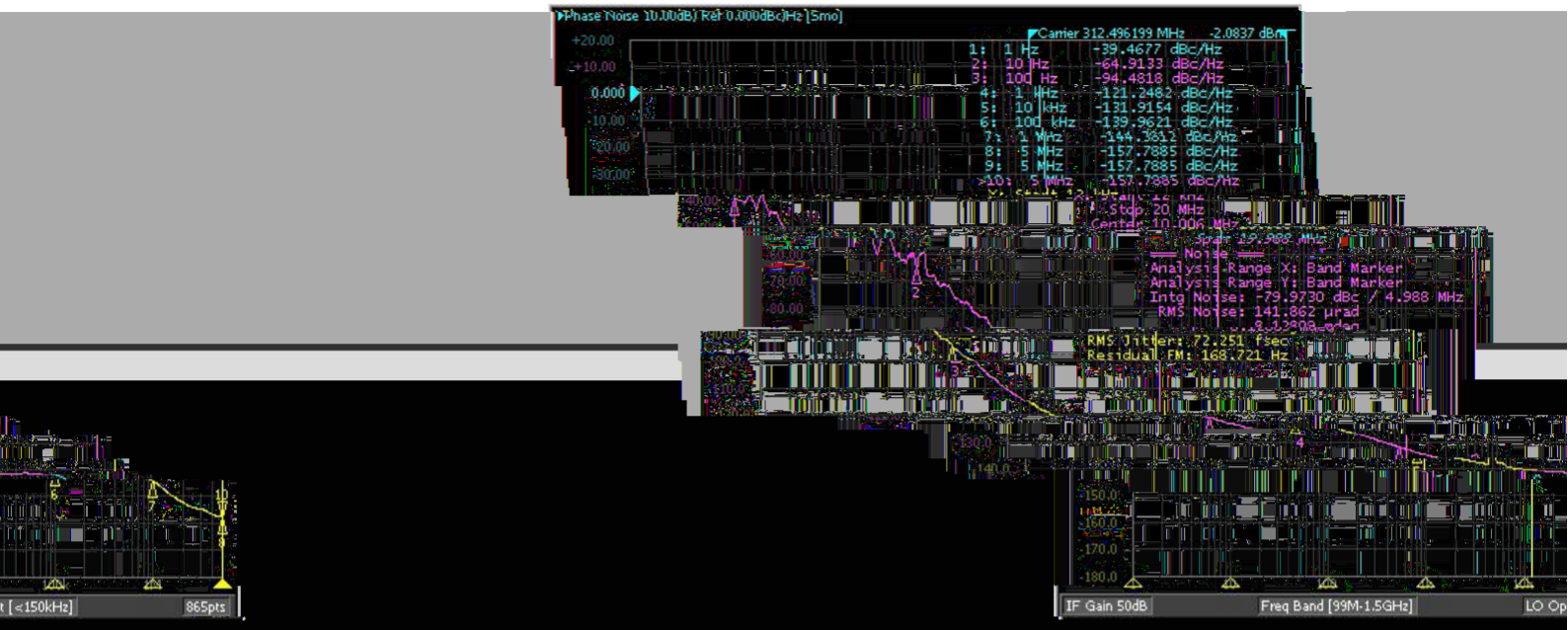



Figure 2 Representative Phase Noise Measurement@312.5M

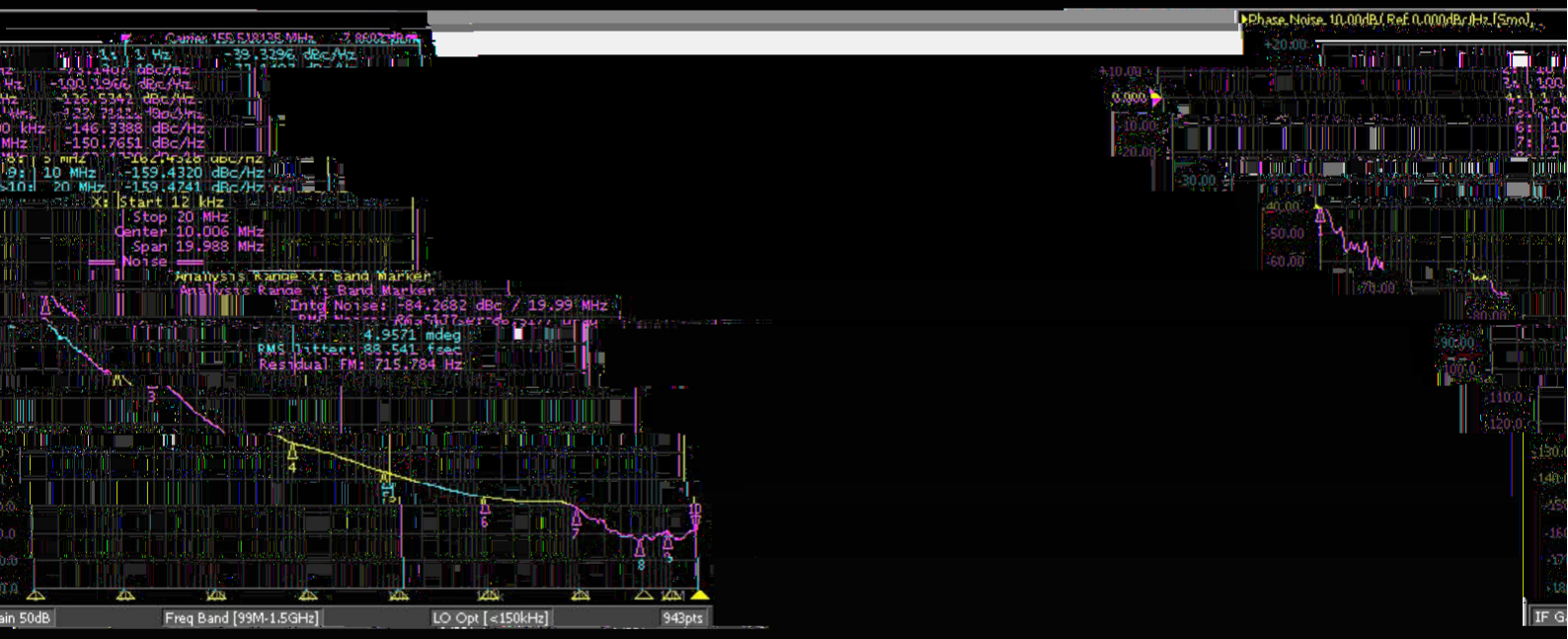



Figure 3Representative Phase Noise Measurement@155.52M

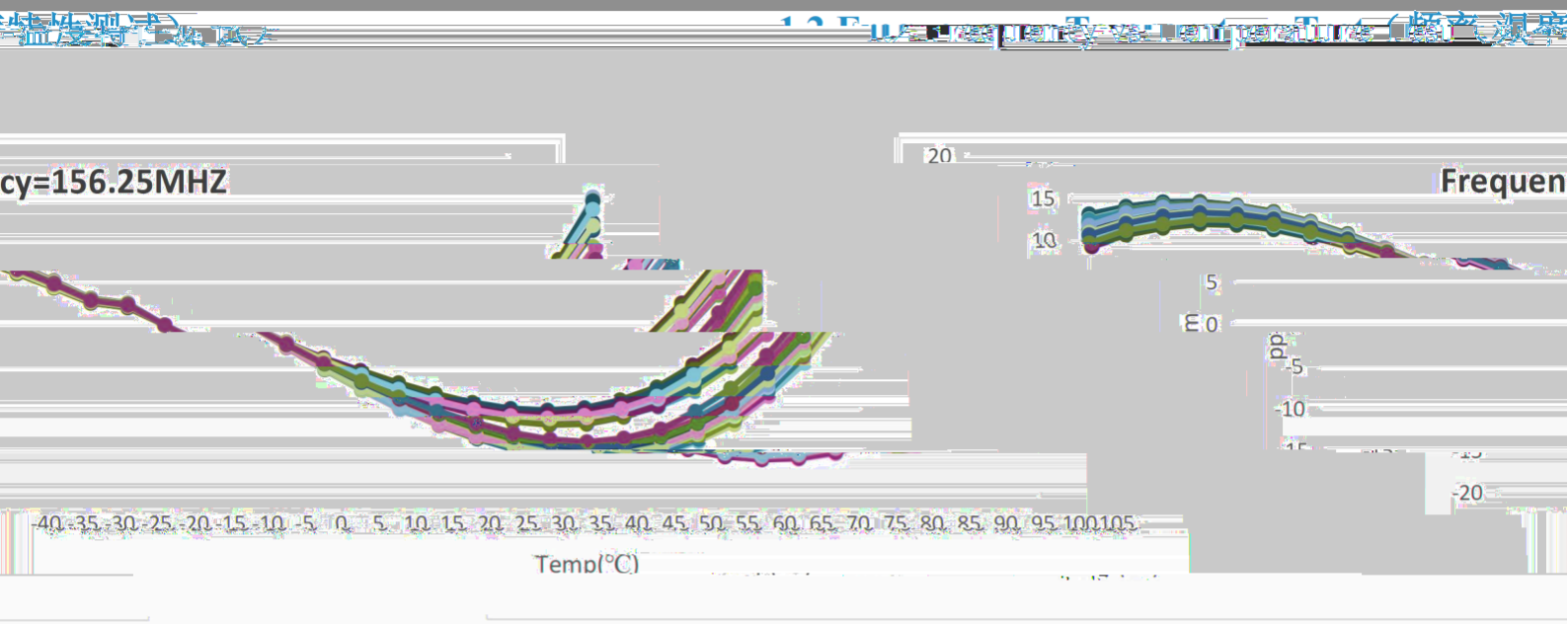



Figure 4 Frequency vsTemperature

## 2 Pin Dimension（脚位尺寸）

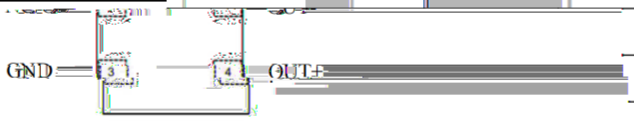




Figure 5 Pin Assignments

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| OE/NC | 2 | Input | Selectable by Ordering Information<br>OE = Output Enable , NC = No connect |
| GND | 3 | GND | GND |
| CLKP | 4 | Output | Clock + f |
| CLKN | 5 | Output | Clock - |
| VDD | 6 | Power | Chip Pow |

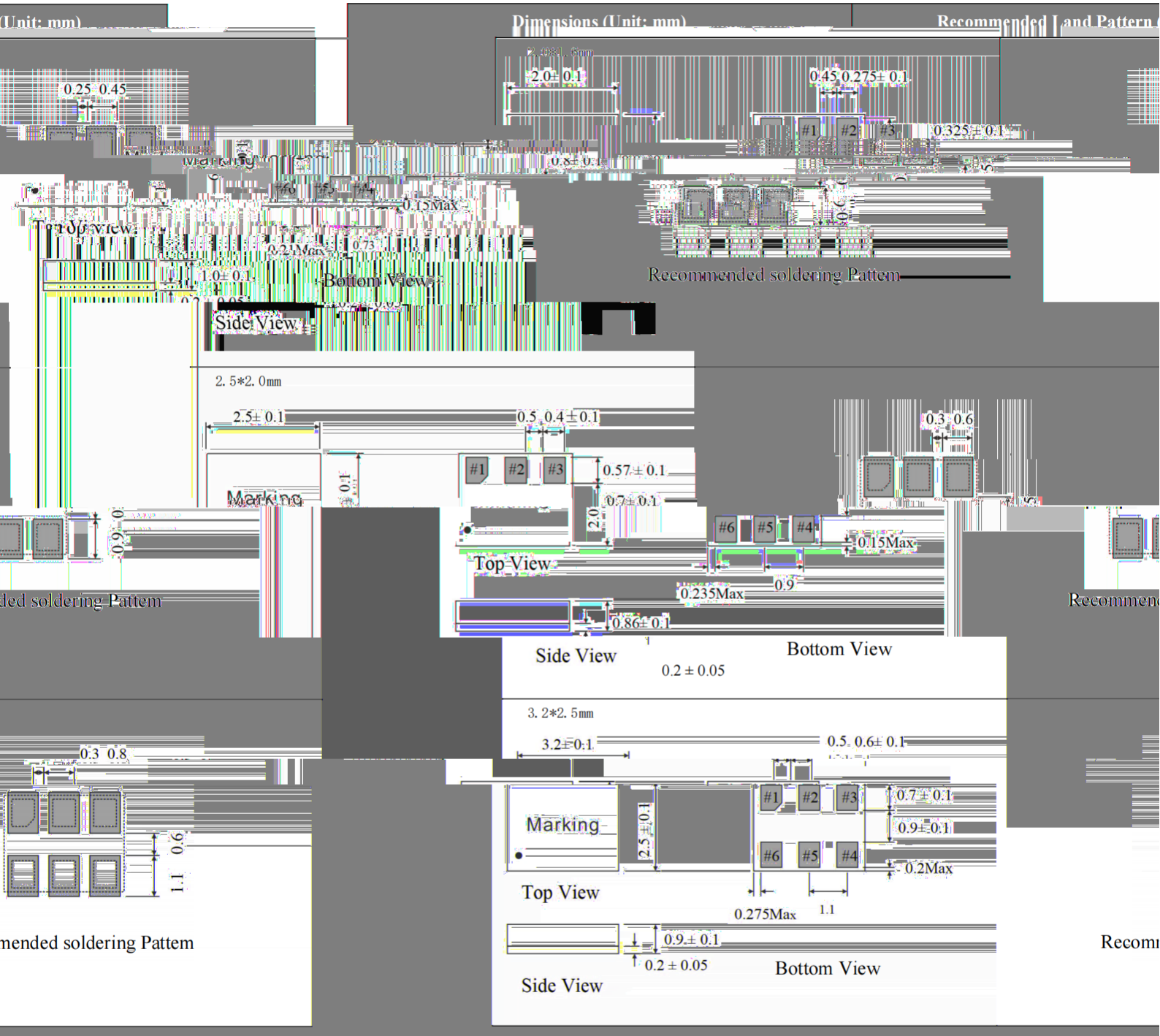
for differential Output.

wer Supply

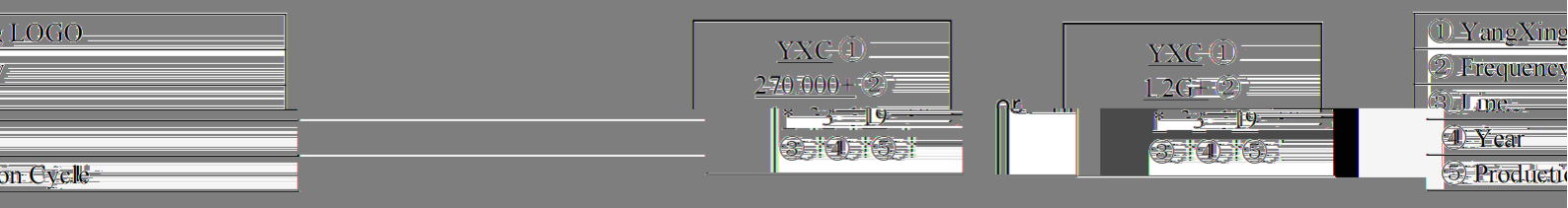
ive High or Low based on the customer requirement.

Notes:The Output Enable Pin can be configured as Acti

## 3 Dimensions and Recommended Land Pattern (尺寸和推荐焊盘)

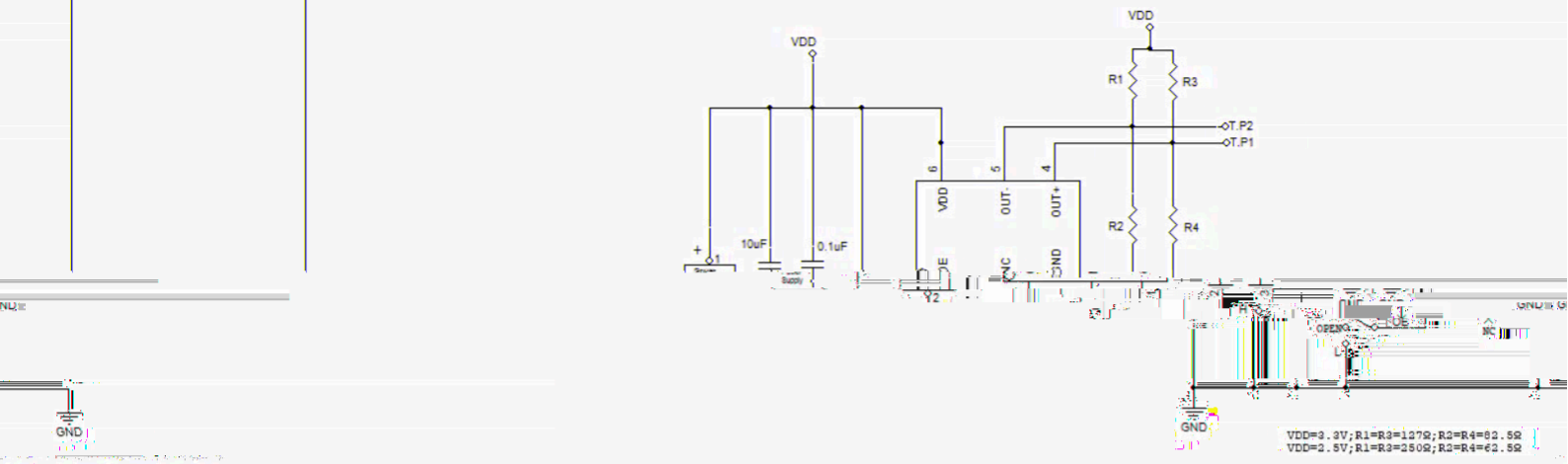



## 4 Marking information (丝印说明)

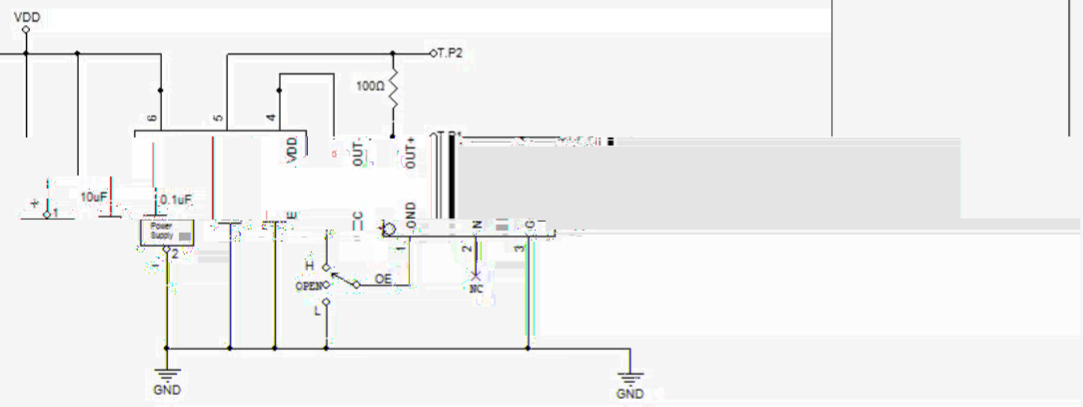


## 5 Test Circuit (测试电路)

### LVPECL




### LVDS/LVDS-Boost




### HCSL/HCSL-LP

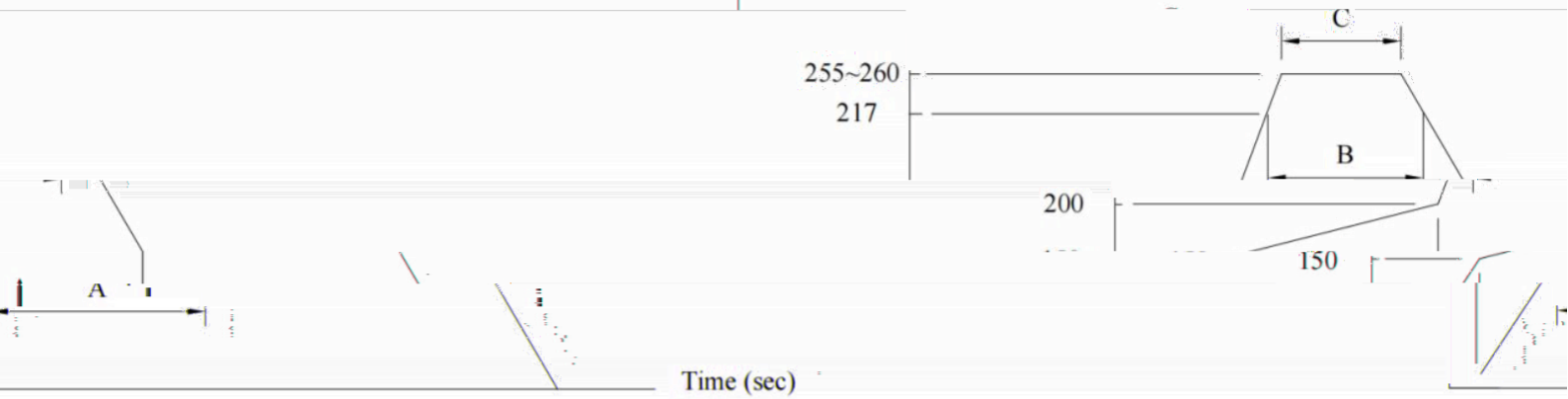



Figure 6. Reflow Profile

(A)→Preheating area : 150~200°C, 60~120sec.

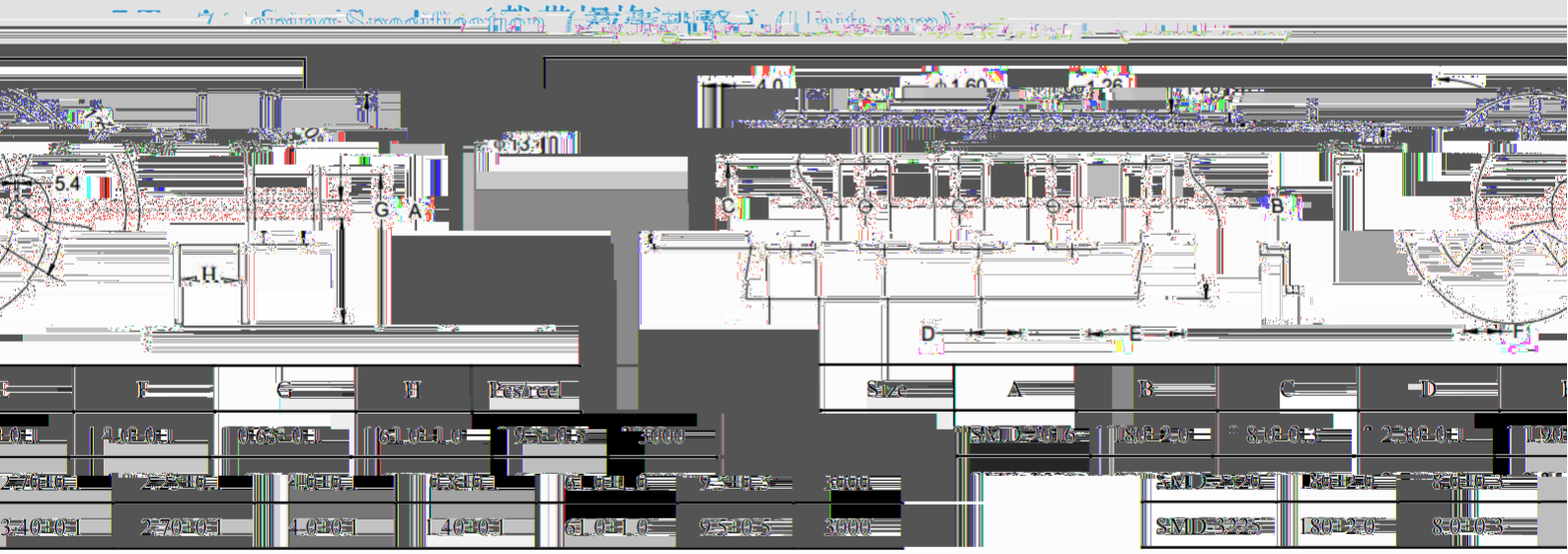
(B)→Heating area : 217°C, 60~150sec.

(C)→Peak temperature : 255~260°C, 30sec. Max.

Ramp-up rate (217→260°C) : 3°C/sec. Max.

Ramp-down rate (260→217°C) : 6°C/sec. Max.

Time 25°C→260°C→80sec. Max.



## 8 Notice（注意）

包装 PACKING

reement.

Packing must prevent damage during transportation and handing. Specific method will be settled by mutual Ag

对环境影响 INFLUENCE TO ENVIRONMENT

This product doesn't use the class ODS at any of production process.

生产厂家 MANUFACTURER

公司名称：深圳扬兴科技有限公司

Shenzhen YangXing Technology Co., Ltd

其它 OTHERS

We guarantee that quartz crystal unit satisfies this specification. If you need the data, we will provide it.

3.如需应用于超声波环境下，请与我们联系。

For application in ultrasone environment, please contact us.

4.变更与联络（MODIFY AND CONTACT）

When the quality is changed due to the changes of the design, technology, material, manufacture place, main equipment and workers, we will first supply the modified products and obtain approval from you, then start to supply mass production.

5.售前售后服务（AFTER SALE SERVICE）

If the defection product was found in the production process, we will exchange and provide the improving measures in time.

This specification is for reference only. If needed, please request a formal letter of acknowledgment from our side to serve as the basis for material acknowledgment and quality judgment.